PVP 12

Code: EC5T5

III B.Tech - I Semester – Regular Examinations - November 2015

DIGITAL IC APPLICATIONS
(ELECTRONICS & COMMUNICATION ENGINEERING)

Duration: 3 hours Max Marks: 70

Answer any **FIVE** questions. All questions carry equal marks

1 a) Explain the various data types supported by VHDL. Give the necessary examples. 7 M

b) Discuss about packages and bindings in VHDL. 7 M

2 a) Explain the data-flow design elements of VHDL. 7 M

b) Design the logic circuit and write a data flow style VHDL program for the following function. 7 M

$$F(p) = \Sigma_{A,B,C,D}\,(2,6,7,9,11,15)$$

3 a) Compare CMOS, TTL with reference to logic levels, DC Noise margin, propagation delay and fan-out. 8 M

b) Design a CMOS transistor circuit for 2 input NAND gate with the help of the function table and explain the circuit. 6 M

4 a) Implement 4x16 decoder using 3 x 8 decoders (IC 74LS138) and other logic gates. 7 M

b) Design a 32 X 1 multiplexer using 8x1 multiplexer (IC 74LS151) 7 M

5 a) Design a full adder using two half adders. Write VHDL data flow program for the same. 7 M

b) Design a 4 X 4 combinational multiplier and then write the necessary VHDL program in data flow model. 7 M

6 a) Explain the operation of simple floating point encoder. 8 M

b) Write a VHDL Code for 8 Bit Comparator. 6 M

7 a) Draw the logic diagram of 74 X 194 and explain the operation. 7 M

b) Design a 4-bit up/down ripple counter with a Control for up/down counting. 7 M

8 a) Compare the static and dynamic RAM's. 7 M

b) With the help of timing waveforms, explain read and write operations of SRAM. 7 M